Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-19. (Canceled).

20. (Currently Amended) A Field Programmable Gate Array ~~reconfigurable~~ device that is configurable ~~for data processing via a method of reconfiguration~~ during runtime, comprising:

a plurality of ~~processing array elements~~ configurable cells that are configurable ~~reconfigurable at a runtime~~ by configuration information;

a ~~plurality of~~ configurable ~~data busses~~ interconnect structure adapted to transmit data in an at least two-dimensional ~~a multi-dimensional~~ way, at least some of the plurality of ~~processing array elements~~ configurable cells being configurable for connection to said ~~busses~~ interconnect structure ~~to provide non-next-neighbor connections~~, wherein said at least some ~~processing array elements~~ configurable cells include units for arithmetic ~~and logic~~ operations, at least one of the [[units]] configurable cells that include units for arithmetic operations including:

an ~~a stage for~~ arithmetic ~~operations~~ operation unit, the [[stage]] arithmetic operation unit including a multiplier stage and an adder stage;

at least three inputs ~~one input~~ and at least one output for data;

~~a first plurality of~~ at least three input registers;

at least one output register;

a return path; and

at least one multiplexer; ~~an element for configuring and reconfiguring;~~ and

an interconnection selection unit ~~element~~ adapted to selectively interconnect said at least one of the [[units]] configurable cells with others of the [[units]] configurable cells;

wherein:

the at least three input ~~a first subset of said first plurality of~~ registers ~~is provided for said at least one input~~ and the at least one output ~~and allows~~ register allow for decoupling of the at least three inputs and the ~~one of said~~ at least one ~~input and said at least one~~ output from said interconnect ~~busses~~ by storing of

operand inputs, the decoupling supporting at least one of pipelining and a decoupling during configuration;

said multiplier stage is connectable to: (a) at least two of the input registers ~~of said first subset~~ for receiving an input of two operands; and (b) said adder stage, said connections to (a) and (b) being such that a selection can be made between at least two of:

(i) adding the two operand inputs;

(ii) adding an output of said multiplier stage and a further operand input;

(iii) adding the output of said multiplier stage and results of the at least one [[unit]] of the configurable cells; and

(iv) adding (a) one of the operand inputs and ~~an output of a result~~ (b) at least one of the results of the at least one [[unit]] of the configurable cells;

said return path is adapted to return said results ~~a result~~ of said at least one [[unit]] of the configurable cells from [[an]] the at least one output register ~~of said first subset~~ as an operand via said at least one multiplexer, said at least one multiplexer [[for]] selecting for further processing one of an external operand input and ~~a result~~ said results; and

said at least one multiplexer is arranged between at least one of said [[an]] input registers ~~register of said first subset~~ and said adder stage so as to allow said at least one of the configurable cells [[unit]] to selectively have direct access to its own results which are returned as operands for calculations in a serial manner ~~; said at least one adder stage is bypassable by allowing for an addition of a zero as one operand input ; said plurality of processing array elements are partially reconfigurable at run time in their function; and the function and interconnection of said plurality of processing array elements are programmed in components specifically accessible by the element for configuring and reconfiguring~~.

21. (Currently Amended) The ~~reconfigurable~~ device of claim 20, wherein the at least one ~~said plurality~~ of the configurable cells is ~~processing array elements are partially reconfigurable~~ configurable at run time in at least one of its [[their]] interconnection and its function.

22. (Currently Amended) The ~~reconfigurable~~ device of claim [[21]] 20, wherein ~~at least some registers of~~ the arithmetic operation unit of the at least one of the configurable cells provides ~~reconfigurable device are shift registers that provide~~ shift capabilities.

23. (Currently Amended) The ~~reconfigurable~~ device of any one of claims 20 and [[claim]] 22, wherein said ~~plurality of processing array elements includes at least one array element having an~~ units for arithmetic ~~and logic unit, a bus access from a data processing in said arithmetic and~~ operations include units for logic ~~unit being decoupled via registers so that said at least one array element is independently functional~~ operations.

24. (Currently Amended) The ~~reconfigurable~~ device of claim [[23]] 20, further comprising:

an element for configuring and reconfiguring, the element transmitting to ~~a second plurality of registers which communicate with~~ the at least one ~~unit for storing~~ of the configurable cells data relating to a configurable function of the at least one [[unit]] of the configurable cells and data relating to an interconnection of stages within the at least one [[unit]] of the configurable cells.

25. (Currently Amended) The ~~reconfigurable~~ device of claim [[24]] 20, further comprising:

~~wherein~~ an element for configuring and reconfiguring, said element for configuring and reconfiguring [[is]] being adapted ~~configured~~ for [[:]] accessing specific registers ~~of said second plurality of registers~~ for at least one of:

storing the data relating to the configurable function;

selectively transferring to said specific registers the data relating to the configurable function; and

selectively transferring to said specific registers the data relating to the configurable interconnection.

26. (Currently Amended) The ~~reconfigurable~~ device of claim [[25]] 24, wherein the data relating to the configurable function of and the interconnection of stages within the at least one [[unit]] of the configurable cells forms a configuration vector that is set through a function control interface and refers to a number of possible instructions, said possible instructions being such that, for any one of the number of possible instructions, a response of any one of the at least some of the plurality of configurable cells ~~processing array elements~~ to said data that refers to the number of possible instructions is identical to a response of any other of the at least some of the plurality of configurable cells ~~processing array elements~~ to said number of possible instructions, said responses remaining the same over time such that transmitted ones of the number of possible instructions statically correspond to a constant one of possible operations.

27. (Currently Amended) The ~~reconfigurable~~ device of claim 20, wherein:

a function and interconnection of the at least one the configurable cells are programmed in registers ~~components~~ specifically accessible by [[the]] an element for configuring and reconfiguring ~~are registers~~.

28. (Currently Amended) The ~~reconfigurable~~ device of claim 27, wherein the ~~reconfigurable~~ device is adapted for reconfiguring said plurality of ~~processing array elements~~ configurable cells in their function and interconnection at run time such that data processing by at least some of said plurality of ~~processing array elements~~ configurable cells is not inhibited while data relating to a configurable function of and an interconnection of stages within another of said plurality of ~~processing array elements~~ configurable cells is transferred to ones of the specifically accessible registers.

29. (Currently Amended) The ~~reconfigurable~~ device of claim 28, wherein a register decoupling from a bus of said ~~other processing array elements~~ another configurable cell when said another ~~processing array element~~ configurable cell is reconfigured by the ~~reconfiguration~~ configuration information at runtime allows for the reconfiguration of said another ~~processing element~~ configurable cell without an interfering effect on data transmitters and receivers in the at least some of said plurality of ~~processing array elements~~ configurable cells, such that ~~: said plurality of processing array elements are partially reconfigurable; and~~ the at least some of said plurality of ~~processing array elements~~ configurable cells are able to continue their data processing during the ~~partial~~ reconfiguration.

30. (Canceled).

31. (Currently Amended) The ~~reconfigurable~~ device of claim 20, wherein said at least some ~~processing array elements~~ configurable cells output, as a status signal, at least one of a carry-over signal, a A<B signal, and a zero signal, wherein A and B are the two operand inputs.

32. (Currently Amended) The ~~reconfigurable~~ device of claim 20, further comprising:

a plurality of configuration registers storing configuration information; and

a configuration multiplexer, wherein at least one of the configuration registers is selected via the configuration multiplexer for a reconfiguration of the plurality of ~~processing array elements~~ configurable cells at runtime.

33. (Currently Amended) The ~~reconfigurable~~ device of claim 32, further comprising:

a selection device that outputs selection data that controls a selector setting of the configuration multiplexer, wherein which of the configuration registers is selected depends upon the selector setting.

34. (Currently Amended) The ~~reconfigurable~~ device of claim 33, wherein the selection device is a counter.

35. (Currently Amended) The ~~reconfigurable~~ device of claim 33, wherein the selection device traverses through a data sequence, the selection data that is output by the selection device depending upon a current point within the traversal.

36. (Currently Amended) The ~~reconfigurable~~ device of claim 33, wherein the configuration registers are associated with respective bits, each bit indicating a respective subsequent configuration to be loaded, the selection device outputting the selection data according to the bits.

37. (Currently Amended) The ~~reconfigurable~~ device of claim 33, wherein the configuration registers are associated with respective flags, each flag indicating a respective subsequent configuration to be loaded, the selection device outputting the selection data according to the flags.

38. (New) The device of claim 20, wherein the at least one of the configurable cells is configurable at run time in its function.

39. (New) The device of claim 22, wherein the function and interconnection of the at least one the configurable cells are programmed in components specifically accessible by an element for configuring and reconfiguring.